Chulkyu Park, Seunghun Song, and Joongho Choi  
*University of Seoul, Korea*

**CDC(P)-154**  
**SIMD Based Multi-Core Architecture for Real-Time Image Processing**  
Junsang Seo, Yonghun Park, Inkyu Jeoung, Myeongsu Kang, and Jong-Myon Kim  
*University of Ulsan, Korea*

**CDC(P)-155**  
**All-Digital On-chip Process Sensor using Ratioed Inverter Based Ring Oscillator**  
Young-Jae An, Dong-Hoon Jung, Kryungho Ryu, and Seong-Ook Jung  
*Yonsei University, Korea*

**CDC(P)-156**  
**An Implementation of Gbps level PHY Transmitter Using 65nm CMOS Technology**  
Hyunsub Kim and Jaeseok Kim  
*Yonsei University, Korea*

**CDC(P)-157**  
**Optimized Intra Prediction for real-time HEVC Encoder**  
Youngjo Kim, Kyungmook Oh, and Jaeseok Kim  
*Yonsei University, Korea*

**CDC(P)-158**  
**Fast-Lock Delay-Locked Loop Using Cyclic-Locking Loop with Duty-Cycle Correction for DRAM**  
Dong-Hoon Jung, Young-Jae An, Kryungho Ryu, Jung-Hyun Park, and Seong-Ook Jung  
*Yonsei University, Korea*

**CDC(P)-159**  
**A bandwidth-tunable optical receiver**  
Kang-Yeob Park, Hyun-Yong Jung, and Woo-Young Choi  
*Yonsei University, Korea*

**CDC(P)-160**  
**A Learning Neuromorphic IC Using Leakage Current**  
Hwa-Suk Cho, Byungsub Kim, Hong-June Park, and Jae-Yoon Sim  
*Pohang University of Science and Technology (POSTECH), Korea*

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**CDC Demo Session**

09:00~17:00 Lobby  
Chair: Kwang Hyun Baek (Chung-Ang University, Korea)  
Kyoung Rok Cho (Chungbuk National University, Korea)

**CDC(D)-1**  
**Design of the Floor Plane Removal System for Motion Recognition Using Depth Images**  
Geun-Jun Kim, Kyounghoon Jang, Hosang Cho, and Bongsoon Kang  
*Dong-A University, Korea*

**CDC(D)-2**  
**CMOS RF Energy Harvesting Rectifier using Parasitic Capacitance Compensation Technique and Low-Pass Filter**  
Junsik Park, Jaeyeon Kim, Seungwook Lee, Phirun Kim, and Yongchae Jeong  
*Chonbuk National University, Korea*

**CDC(D)-3**  
**A Prototype for Estimating SoC in the Battery-powered Mobile System**  
Minsu Oh and Hyunjin Kim
CMOS RF Energy Harvesting Rectifier using Parasitic Capacitance Compensation Technique and Low-Pass Filter

Junsik Park, Jae Yeon Kim, Seungwook Lee, Phirun Kim, and Yongchae Jeong
Chonbuk National University, Republic Of KOREA

I. INTRODUCTION
Currently, RF energy harvesting technology has become an interesting research issue for one of the eco-friendly energy reusing technologies. If RF energy harvesting system using CMOS process technology is applied into power transmission terminal and wireless communication, it will be great help to overcome the problem of battery efficiency. Since the RF energy floating in the air is the power of -30 dBm or less, generally it is not sufficient power to operate rectifier circuit in the RF energy harvesting system. Therefore, generally the rectifier circuit uses a Schottky diode having a low threshold voltage to minimize the loss of voltage and efficiency. However, the implementation of RF energy harvesting system using the Schottky diodes in CMOS process is difficult due to manufacturing cost and process technology. Therefore, the different design and research direction is necessary.

II. DESCRIPTION
Fig. 1 shows the schematic of the proposed on-chip RF harvesting rectifier using a 0.11 um CMOS process. In this work, the rectifier circuit is a Villard voltage doubler structure using a diode connection MOSFET. The PMOS has a floating body structure in order to reduce body effect losses. Since the parasitic capacitance of MOSFET can cause the degradation in conversion efficiency, it is necessary to compensate these parasitic components. For this purpose, the inductor was used which can provide a form of virtual series resonant circuit with parasitic capacitance of both transistors. Furthermore, it is possible to increase the conversion efficiency by suppressing the harmonic components generated by the MOSFET and flattening DC signal using an off-chip low pass filter. The load resistor value was optimized for maximum conversion efficiency.

Fig. 1. Proposed RF energy harvesting rectifier circuit

III. CHIP IMPLEMENTATION AND RESULTS
Fig. 2 shows the die photo of the proposed on-chip RF harvesting rectifier. The whole chip area is 1280 × 780 um², including bonding pads. Fig. 3 (a) and (b) show the measured return loss (S11) characteristic, conversion efficiency and output DC voltage, respectively. From the result, the return loss is better than -12 dB in overall operating bandwidth. Efficiency of 15% or more is obtained for an input power of 7–20 dBm which can significantly affect in battery efficiency enhancement of near field communication systems.

Fig. 2. Die photo of the proposed RF energy harvesting rectifier

Fig. 3. Measurement result (a) Return loss characteristic (b) Output DC voltage and conversion efficiency

REFERENCE